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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,134	04/04/2001	David K. Vavro	INTL-0546-US (P11105)	2324

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/826,134	VAVRO, DAVID K.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ishida et al., US Patent 5,293,500 (hereinafter Ishida).

3. Referring to claim 1, Ishida has taught a method comprising:

a. providing a register accessible by a plurality of central processing units (abstract, column 2, lines 3-23, Figures 1-13, Figure 9, element 506); and

b. indicating whether data in said register is available for a given central processing unit (abstract, column 2, lines 3-23, Figures 1-13, Figure 9, element 108).

4. Referring to claim 2, Ishida has taught the method of claim 1, as described above, and including indicating for each of a plurality of central processing unit whether the data is available for a given central processing unit (abstract, column 2, lines 3-23, Figures 1-13).

5. Referring to claim 3, Ishida has taught the method of claim 2, as described above, and including requiring a central processing unit to wait to execute an instruction until the data it needs to execute the instruction is available in one or more registers (column 8, lines 39-44).

6. Referring to claim 4, Ishida has taught the method of claim 3, as described above, and including providing a bit for each item of data indicating whether a given central processing unit can access that data (column 4, lines 18-25).

7. Referring to claim 5, Ishida has taught the method of claim 4, as described above, and including resetting said bit when said data is accessed by a given central processing unit (column 4, lines 18-25).

8. Referring to claim 6, Ishida has taught the method of claim 5, as described above, and including providing a register with a bit for each of a plurality of central processing units (abstract, column 2, lines 3-23, Figures 1-13, column 4, lines 18-25, the register scoreboard bits are for each CPU.), enabling a central processing unit to reset said bit when the data is no longer useful to the processor (column 4, lines 18-25), and preventing any central processing unit from writing data to said register until all of the bits indicate that the data is no longer useful to any other central processing unit (column 4, line 9-column 6, line 66).

9. Referring to claim 7, Ishida has taught the method of claim 6,as described above, and including indicating the central processing unit which will utilize the data written into the register (column 4, line 9-column 6, line 66).

10. Referring to claim 8, Ishida has taught the method of claim 1, as described above, and includes enabling a plurality of central processing unit s to access a register at the same time (column 6, lines 26-32).

11. Referring to claim 9, Ishida has taught the method of claim 1, as described above, and including providing specialized central processing unit s for mathematical operations and for memory (column 7, lines 23-36, column 3, lines 14-29).

12. Referring to claim 10, Ishida has taught the method of claim 1, as described above, and including providing an input central processing unit (Figures 1-13, All of the processors input data.), an output central processing unit (Figures 1-13, All of the processor output data.) and

coupling said input, output and specialized central processing units to said register through a cross-bar connection (Figures 1-13, All of the processors have the ability to send data to one another through the register files using a priority scoreboard.).

13. Claims 11-17 do not recite limitations above the claimed invention set forth in claims 1-7, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 1-7 above.

14. Referring to claim 18, Ishida has taught a digital signal processor including:

a. a plurality of central processing units (figure 2, elements 11 and 15, Figures 3 and 4, elements 11 and 15, figure 6, elements 59 and 60, Figure 9, elements 106 and 107, etc.); and

b. a register coupled to said plurality of processing units, said register including a plurality of general purpose registers each accessible by said plurality of processing units (abstract, column 2, lines 3-23, Figures 1-13, elements 12, 13, 74, and 506), at least one of said registers indicating whether data in said register is available for a given one of said plurality of processing units (abstract, column 2, lines 3-23, Figures 1-13, elements 14, 63, 108, and 507).

15. Claims 19, 20, 21, 22, and 23 do not recite limitations above the claimed invention set forth in claims 10, 12, 3, 4, and 6, respectively, and are therefore rejected for the same reasons set forth in the rejection of claims 10, 12, 3, 4, and 6 above.

16. Referring to claim 24, Ishida has taught the processor of claim 18, as described above, and including a plurality of general purpose registers, each of said general purpose registers including a data section (abstract, column 2, lines 3-23, Figures 1-13, elements 12, 13, 74, and

506) and a storage area for a bit for each of said plurality of processing units (abstract, column 2, lines 3-23, Figures 1-13, elements 14, 63, 108, and 507, column 4, lines 18-25).

17. Referring to claim 25, Ishida has taught the processor of claim 18, as described above, and wherein said general purpose register is accessible by each of said processing units at the same time (column 6, lines 26-32).

18. Claim 26 does not recite limitations above the claimed invention set forth in claim 19 and is therefore rejected for the same reasons set forth in the rejection of claim 19 above.

19. Referring to claim 27, Ishida has taught the processor of claim 26, as described above, and further including at least one multiply (column 1, lines 22-38) and accumulate (column 1, lines 22-38, column 7, lines 24-36) processing unit.

20. Referring to claim 28, Ishida has taught the processor of claim 27, as described above, and including at least one processing element for storing data in a random access memory (column 4, line 46-column 6, line 67).

21. Referring to claim 29, Ishida has taught the processor of claim 18, as described above, and wherein no master processing element is included and instead, the sequence of operations in said digital signal processor is driven by the availability in a general purpose register of data needed to execute instructions (column 6, lines 13-67).

22. Referring to claim 30, Ishida has taught the processor of claim 18, as described above, and including a plurality of special purpose processing units that may each access a register at the same time (column 6, lines 26-32).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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